result of this summation is equalized sequence $s_5[n]$, 506. The sequence 506 is fed to a symbol detector 503 that employs a memoryless nearest neighbor decision rule, based on the transmitted symbols' I-Q constellation to generate the sequence â[n]. We note that in this preferred embodiment, a single memoryless decision rule is employed. However, the present invention can be employed in a receiver that employs a more accurate detection scheme such as an approximate nearest sequence detector which is the maximum likelihood sequence estimator when the noise of the input of unit 503 has a Gaussian distribution.

OATH/DECLARATION:

The Office Action states that "[t]he oath or declaration is defective because: The signature of the second named inventor is not in permanent ink, or its equivalent in quality . . . ." Applicants believe that the signature was executed properly and respectfully requests the Examiner further elaborate on the problem with the signature or withdraw this objection.

IN THE DRAWINGS:

Please replace the Figure 4 with the new corrected drawing which adds the reference sign mentioned in the description. The corrected drawing is included herewith. No new matter is added.

IN THE CLAIMS:

Please amend claims 1, 16, 17, and 20 as follows:

1. (amended) A communication receiver, comprising:

an input receiving a modulated analog signal containing digital information;

a front end unit operable for performing analog to digital conversion, for performing demodulation and for performing timing control, and further operable for

producing a demodulated complex-valued digital signal from the modulated analog signal;

a digital equalizer connected for receiving the demodulated complex valued digital signal, comprising:

A2 cont'd

a first filter operable for receiving the demodulated complex valued digital signal;

a second filter connected to the first filter and operable for reducing the amount of noise and inter symbol interference in the demodulated complex valued digital signal without the use of training data; and

a symbol-to bit converter connected to the second filter.

Sub B1

16. (amended) A digital communication receiver, comprising:

a input stage receiving an analog signal containing digital information;

an analog to digital converter connected for producing a complex-valued digital signal from the modulated analog signal;

a demodulator connected for producing a demodulated complex-valued digital signal from the complex-valued digital signal;

a pre-equalizer filter connected to receive the demodulated complex-valued digital signal, comprising:

A3 cont

a first adaptive finite response filter having an output, having a tap adjustment input and connected to receive the demodulated complex-valued digital signal;

a first summation circuit connected to sum the demodulated complex-valued digital signal with the output of the first adaptive finite response filter to produce a pre-equalized complex-valued signal;

a function circuit connected to receive the pre-equalized complex-valued signal and operable for producing there from a non-linear response to the pre-equalized complex-valued signal;

an adaptation unit connected to receive the demodulated complex-valued digital signal, connected for receiving the non-linear response and connected to

the tap adjustment input of the adaptive finite response filter to provide an adjustment to the first adaptive finite response filter;

a digital decision feedback equalizer connected to receive the pre-equalized complex-valued signal, comprising:

a rotator having an adaptive input and connected to receive the pre-equalized complex-valued signal and operable for restoring the phase of input data contained in the pre-equalized complex-valued signal without the use of training data;

a feed forward equalizer finite input response filter having an adaptive input, an input connected to the rotator, an output, and operable for adaptively reducing the amount of noise and inter-symbol interference in the pre-equalized complex-valued signal without the use of training data;

a second summation circuit connected to sum the output of the feed forward equalizer finite input response filter with the output of a second adaptive finite response filter and for producing therefrom a corrected complex-valued signal;

#13 cont

a symbol detector connected to receive the corrected complex valued signal and to produce a symbol signal;

the second adaptive finite response filter having an output, an adaptive input and connected to receive the symbol signal;

wherein the corrected complex-valued signal is connected to the adaptive input of the rotator, the adaptive input of the feed forward equalizer finite input response filter and the adaptive input of the second adaptive finite response filter; and

a symbol-to-bit converter connected to receive the symbol signal and to produce therefrom digital bits corresponding to the digital information.

Sub B17

17. (amended) A method of receiving a digital communication signal in the presence of inter-symbol interference, comprising the steps of:

receiving an analog signal modulated with digital information;

converting the analog signal to produce a digital signal;

multiplying the digital signal with sine and cosine signals to produce a complex-valued digital signal;

A3 Cancel

adaptively pre-equalizing the complex-valued digital signal to produce a pre-equalized complex-valued digital signal;

adaptively equalizing the pre-equalized complex-valued signal to reduce the inter-symbol interference and to produce a corrected complex valued symbol signal without the use of training data; and

converting the corrected complex valued symbol signal to the digital information.

Sub B1

20. (amended) A communication system, comprising:

a digital communications transmitter;

a communications medium; and

a digital communications receiver, comprising:

a input receiving a modulated analog signal containing digital information;

an analog to digital converter connected for producing a complex-valued digital signal from the modulated analog signal;

A4

a demodulator connected for producing a demodulated complex valued digital signal from the complex valued digital signal;

a digital equalizer connected for receiving the demodulated complex valued digital signal, comprising:

a first filter operable for receiving the demodulated complex valued digital signal;

a second filter connected to the first filter and operable for reducing the amount of noise and inter symbol interference in the demodulated complex valued digital signal without the use of training data; and

a symbol-to bit converter connected to the second filter.
